

CLAIMS

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- 1 1. A source synchronous link comprising:
- 2 a communication link;
- 3 a source synchronous receiver coupled to said communication link; and
- 4 a source synchronous transmitter coupled to said communication link, including,
- 5 data transmit logic configured to manage the transmission of data signals
- 6 over a data line of said communication link; and
- 7 data strobe transmit logic configured to generate a one or more data strobe
- 8 signals over a clock line of said communication link, wherein said data strobe
- 9 transmit logic halts each said one or more data strobe signals in a logical state in
- 10 response to an external condition.
- 1 2. The source synchronous link of claim 1, wherein said one or more data strobe
- 2 signals comprise a first data strobe signal and a second data strobe signal transmitted
- 3 with a phase opposite a phase of said first frequency.
- 1 3. The source synchronous link of claim 1, wherein said first data strobe signal and said
- 2 second data strobe signal may be transmitted at either one of two logical states and
- 3 wherein said data strobe transmit logic maintains said first data strobe signal at a first of
- 4 said two logical states and maintains said second data strobe signal at a second of said
- 5 two logical states when said data strobe transmit logic halts said one or more data strobe
- 6 signals.
- 1 4. A source synchronous transmitter constructed and arranged to transmit a differential
- 2 data strobe over a source synchronous link at a first frequency, with the differential data
- 3 strobe signals toggling between one of two logical states at said first frequency when
- 4 operating in a normal mode of operation and with the differential data strobe signals held
- 5 at one of the logical states when operating in a data capture debug mode of operation.

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- 1 5. A debug system to determine whether source synchronous receiver has properly
2 captured data transmitted from a transmitter, comprising:
3 a source synchronous transmitter;
4 a source synchronous receiver;
5 a debug system configured to control said transmitter to transmit data and a data strobe at
6 a first frequency and to transmit a debug bit pattern while holding said differential data
7 strobe at a predetermined logic level;
8 a data capture storage and analysis device configured to scan said receiver to retrieve and
9 store captured data for comparison with said debug bit pattern.

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1 6. The source synchronous link of claim 4, wherein said transmitter comprises:
2 a differential data strobe transmit logic configured to generate said differential data
3 strobe comprising a data strobe signal and an inverse data strobe signal;
4 a differential data strobe signal generator configured to determine a said logical states of
5 said data strobe and said inverse data strobe signals;
6 a strobe stopping logic that controls said logic level signals utilized by said signal
7 generator to cause said data strobe and said inverse data strobe signals to remain halted in
8 a desired logical state.

- 1 7. In a source synchronous communication system, a method for determining whether a
2 source synchronous link receiver properly captured data transmitted by a source
3 synchronous transmitter, the method comprising the steps of:
4 a) transmitting by the transmitter a data signal at a first clock frequency;
5 b) transmitting by the transmitter concurrently with said step a), at least one data strobe
6 signal at a second clock frequency, wherein said data strobe signal alternates between a
7 high logical state and a low logical state during each data strobe cycle;
8 c) receiving, by the transmitter, a command to halt the data strobe signal; and
9 d) maintaining, by the transmitter in response to said command, said one or more data
10 strobe signals transmitted by said transmitter at one logical state.

1 8. The method of claim 7, further comprising the step of:
2 e) prior to said step d), receiving an indication of the logical state in which to maintain
3 said data strobe signal, and
4 wherein said one logical state at which said one or more data strobe signals are held, is
5 said logical state indicated in said step e).

1 9. In a source synchronous system, a method for determining whether a source
2 synchronous receiver has properly captured data transmitted from a source synchronous
3 transmitter, the method comprising the steps of:
4 selecting a bit pattern to transmit over communication link coupling said transmitter
5 and said receiver;
6 causing the transmitter to halt differential data strobe and to transmit concurrently
7 said predetermined bit pattern to the receiver;
8 scanning data capture flip-flops in the source synchronous receiver to retrieve
9 captured bit pattern;
10 storing said captured data; and
11 comparing said captured data with said transmitted bit pattern.

1 10. The method of claim 9, wherein said step of selecting comprises the steps of:
2 writing said predetermined bit patterns to a memory; and
3 retrieving a selected predetermined bit pattern from the memory.

1 11. A differential data strobe transmitter for generating a differential data strobe
2 comprising a data strobe signal and an inverse data strobe signal over a communication
3 link with a data signal, comprising:
4 a differential data strobe signal generator that determines a shape of said data
5 strobe signal and said inverse data strobe signal waveforms; and
6 strobe stopping logic configured to control signal level states used by said signal
7 generator logic to cause said data strobe signal and said inverse data strobe signal to
8 remain halted in a desired logical state.

1 12. The differential data strobe transmitter of claim 11, wherein said differential data
2 strobe signal generator logic selects alternately between two applied signal levels to
3 generate each said data strobe signal and said inverse data strobe signal.

1 13. The differential data strobe transmitter of claim 12, wherein said differential data
2 strobe signal generator receives as inputs a first and a second logic level signal for
3 selection to generate said data strobe signal and a third and fourth logic level signals for
4 selection to generate said inverse data strobe signal.

1 14. The differential data strobe transmitter of claim 12,
2 wherein during normal operations, said differential data strobe is not halted, said
3 first and third input signals are held consistently in an asserted state while said second of
4 fourth input signals are held consistently in a de-asserted state,
5 wherein said signal generator selects alternately said first and said second input
6 signals to generate said data strobe signal at a first clock frequency, and between said
7 third and said fourth input signals to generate said inverse data strobe signal at said first
8 clock frequency.

1 15. The differential data strobe transmitter of claim 12, wherein said data strobe signal
2 and said inverse data strobe signal are each generated as single ended bits that are
3 opposite in phase with each other.

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